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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,039	11/14/2001	Craig Nemecek	CYPR-CD01222M	1791

7590 11/22/2005  
WAGNER, MURABITO & HAO LLP  
Third Floor  
Two North Market Street  
San Jose, CA 95113

EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 11/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/004,039

Applicant(s)

NEMECEK ET AL.

Examiner

Jason Proctor

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06 September 2005.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-19 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 14 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☒ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. 20051115.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

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### **DETAILED ACTION**

Claims 1-19 were rejected in office action dated 6 June 2005. Applicants' response dated 6 September 2005 has amended claim 18. Claims 1-19 have been submitted for reconsideration.

Claims 1-19 have been rejected.

The Amendment after Non-Final Rejection in the record for this application, dated 12 September 2005, appears to be a duplicate submission or scanning error and has been disregarded. Please see attached form PTO-413B.

### ***Oath/Declaration***

The Examiner thanks Applicants for resubmitting the Declaration and Power of Attorney in this application to overcome the previous objections. Those objections have been withdrawn.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 3, and 7-10 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the

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relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 3, and 7 recite a limitation including the phrase “replacing the microcontroller clock with the gatekeeper clock for clocking the virtual microcontroller when a watchdog event occurs” which is inadequately described by the disclosure. The claim seems to imply that the microcontroller clock drives the virtual microcontroller, a connection which is neither recited by these claims nor, in the case of claims 3 and 7, by any claim from which they depend.

In response, Applicants argue primarily that:

Applicants respectfully assert that one having ordinary skill in the art would thus understand from the specification [page 12, ln. 13, through page 13, ln. 18; page 14, ln. 22, through page 15, ln. 17; and page 26, ln. 3, through page 28, ln. 5 specifically cited by Applicants] how to practice embodiments of the invention disclosed in Claims 3, 7, and 15.

The Examiner respectfully traverses this argument as follows.

As an initial matter, the citations in Applicants’ response appear to contain typographical errors regarding several page numbers. The Examiner has attempted to interpret these citations in accordance with Applicants’ arguments. The citations shown above are those interpretations.

The Examiner has carefully considered the portions of the specification relied upon by Applicants’ arguments as well as the specification as a whole and maintains that the claims recite subject matter which is not described in the specification in accordance with 35 U.S.C. § 112. The Examiner does not challenge that the specification describes the four line interface, the clock signals passed, and the operation of the gatekeeper circuit. However, the claim limitations recite, in part:

the gatekeeper circuit further comprises switching means for replacing the microcontroller clock with the gatekeeper clock for clocking the virtual microcontroller when a watchdog event occurs.

MPEP 2111.01 reads as follows:

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[T]he words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) (discussed below)\*\*>; *Chef America, Inc. v. Lamb-Weston, Inc.*, 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004) (Ordinary, simple English words whose meaning is clear and unquestionable, absent any indication that their use in a particular context changes their meaning, are construed to mean exactly what they say.

The ordinary, simple English word “clock” would be recognized by a person of ordinary skill in the art to clearly and unquestionably refer to the tangible device that creates a “clock signal”. Careful consideration of the specification fails to reveal any clear definition in the specification that “clock” is equivalent to “clock signal”; indeed that equivalence would significantly complicate any disclosure regarding clocks and clock signals as in this application. Compare to the language of claim 15, which recites in part:

replacing the microcontroller clock signal with a gatekeeper clock signal to the virtual microcontroller  
Claims 3 and 7 do not recite replacing a “clock signal”, but rather recite “replacing the microcontroller clock”. Nowhere does the disclosure describe “replacing a clock”. Applicants’ arguments have been fully considered but have been found unpersuasive.

2. Claims 3, 7-10, are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 3, and 7 recite a limitation related to gatekeeper circuit switching means for replacing a clock on a microcontroller with a clock from another device. This limitation appears to be directed to physically replacing a tangible component of a tangible microcontroller with a second tangible component from a second tangible device. A person of ordinary skill in the art of software debugging would be unable to make and use an in-circuit emulation system that involves a

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gatekeeper circuit that physically replaces the components of microcontrollers or other electronic devices.

In response, Applicants' argue primarily that:

The rejection contends that Claims 3, 7, and 15 require a physical replacement of one tangible component with a second tangible component. Applicants respectfully submit that no such requirement is set forth in Claims 3, 7, and 15, in either explicit or implied terms. Further, Applicants assert that one having ordinary skill in the art would understand the concept of switching, e.g., multiplexing, as applied to electronic circuits, and would be enabled to practice the embodiments of the present invention recited in Claims 3, 7, and 15.

The Examiner respectfully traverses this argument as follows.

As explained above, the ordinary, simple English terms "replacing the microcontroller clock" explicitly require physical replacement of one tangible component with a second tangible component. Claim 1 (from which claim 3 depends) explicitly recites "a microcontroller having a microcontroller clock". Claim 7 explicitly recites, in part, "the apparatus according to claim 1, further comprising a gatekeeper clock". These explicit recitations require tangible components, specifically "clocks", given the ordinary, simple English definitions of these terms. The concept of "switching, e.g., multiplexing" has not been found in the language of claims 3 or 7. Applicants' argument have been fully considered but have been found unpersuasive.

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 3 and 7-10 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 3 and 7 recite a limitation including the phrase "switching means for replacing the microcontroller clock with the gatekeeper clock for clocking

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the virtual microcontroller when a watchdog event occurs” which at least vague and indefinite. This limitation appears to imply that the microcontroller clock actually drives the virtual microcontroller, however there is no clear recitation of that structure. It is not clear what is meant by replacing a microcontroller clock with the gatekeeper clock. A clock is known in the art as a tangible device which, in the context of microprocessors, generates a periodic pulse signal. A clock is typically incorporated into the design of a computer system and nothing in the disclosure or the claims suggests that Applicants’ invention actually replaces on clock with another clock. It is entirely unclear which clocks are driving what devices as recited by claims 3 and 7. Clarification is respectfully requested.

In response, Applicants’ argue primarily that:

Applicants respectfully assert that one having ordinary skill in the art would understand the use of the term “replacing” to suggest substitution or switching of one clock signal with another, rather than physical replacement of circuitry.

The Examiner respectfully traverses this argument as follows.

Claims 3 and 7 clearly recite replacement of circuitry as explained above. Applicants’ arguments have been fully considered but have been found unpersuasive.

Applicants’ arguments directed toward the previous rejections of claims 15-19 under 35 U.S.C. § 112, have been fully considered and found persuasive. As noted above, claim 15 is directed toward replacing a “clock signal,” which is supported by the disclosure in compliance with 35 U.S.C. § 112. The previous rejections of claims 15-19 under 35 U.S.C. § 112 have been withdrawn.

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The previous rejections of claims 5-6, 9-10, 12-13, and 17-18 under 35 U.S.C. § 112, second paragraph, have been withdrawn in light of Applicants' arguments. The Examiner thanks Applicants for pointing out the description at page 28 of the specification which supports these claims.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependency.

### *Claim Interpretation*

In response to the previous claim interpretation of the phrase "disabling a microcontroller clock signal" in claim 15, Applicants submit that:

No objection was presented in the rejection as to the language of "disabling a microcontroller clock signal," making the origin of and reason for this interpretation unclear.

This interpretation was made without properly acknowledging the language of claim 15, directed to a "clock signal", as opposed to claims 3 and 7 directed to a "clock". The Examiner apologizes for any confusion or inconvenience. The Examiner concurs that claim 15 should be interpreted as presented.

Regarding the interpretations of claims 5, 9, 12, and 17, Applicants submit that:

The rejection further states that, with respect to Claims 5, 9, 12, and 17, the limitations of these Claims are so different from the teachings of the specification that the Examiner cannot interpret them. Applicants understand this statement to be based upon the 35 U.S.C. 112 rejections, discussed above. Applicants respectfully assert that the limitations of these Claims arise directly from the teachings of the specification, as discussed above, rendering moot this interpretation of the language of these Claims.

The Examiner concurs that claims 5, 9, 12, and 17 should be interpreted as presented. The Examiner thanks Applicants for pointing out the description at page 28 of the specification.

The Examiner thanks Applicants for carefully identifying the support for the claims in the disclosure, especially in light of the Request for Non-Publication filed in this application.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,911,059 to Profit, Jr. (Profit).

Regarding claim 1, Profit teaches an in-circuit emulation system including:

A microprocessor (column 6, lines 5-24, especially lines 18-19), the microprocessor has a clock count and therefore a clock (column 12, lines 24-35);

A virtual microprocessor (referred to as a processor model shell 212) (column 6, lines 25-32) running in lock-step with the microprocessor (column 11, lines 40-43);

A host computer running in-circuit emulation debug software (column 6, lines 25-60), the host computer being in communication with the virtual microcontroller (Fig. 7, reference 220; column 5, line 58 – column 6, line 4); and

A gatekeeper circuit (referred to as RUN/HALT controller 240) coupled to the virtual microcontroller and the microcontroller (Fig. 8, reference 240; column 8, line 65 – column 10, line 31) that detects when a watchdog timer (referred to as time keeper circuit 232) expires in the

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microcontroller and notifying the host computer that the watchdog event has occurred (column 10, line 32 – column 11, line 7).

Official Notice is taken that the term microcontroller refers to a single unit usually comprising central processing unit, memory, and I/O ports. As Profit teaches an emulator unit that contains at least these features (Fig. 7, reference 202), it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention that Profit's emulator is readily adaptable to accept microcontrollers, as would be desired by a person whose goal it is to develop and debug code for microcontrollers.

Applicants have not challenged and seasonably traversed this Official Notice.

In response, Applicants' argue primarily that:

Applicant contends that Profit fails to disclose a virtual microcontroller running in lock-step synchronization with the microcontroller, as claimed. Applicant further contends that Profit fails to disclose a host computer running In-Circuit Emulation debug software, as claimed.

[...]

From the example provided, the hardware simulator of Profit is principally a processor model shell, which simulates activity at the target processor's pins; however, it does not emulate the processor's functionality, see col. 6, ln. 25-48. The hardware simulator of Profit is not a virtual microcontroller.

[...]

[T]he portion of Profit referenced to demonstrate In-Circuit Emulation debug software does not disclose the operation of In-Circuit Emulation debug software, but rather states a generalization about what software might be running on the host computer, and provides an example of a software package for designing the target *circuitry*; see col. 6, ln. 49-60.

The Examiner respectfully traverses this argument as follows.

To address Applicants' first argument, Applicants' attention is respectfully drawn to Profit, column 6, lines 27-32, emphasis added:

The hardware simulator 210 is a conventional software program that simulates the electrical and logical activity of the target circuitry as seen by the target processor [*target processor 204 (see column 6, lines 19-24)*]. The hardware simulator 210 includes a **processor model shell 212 which converts a sequence of processor functions to activity at simulated pins of the target processor [*target processor 204*]. Such a sequence of processor functions corresponds to an instruction executed in the target program 22 [...]**

Applicants' attention is respectfully drawn to Profit, column 6, lines 12-15, emphasis added:

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**The processor 204 communicates with the memory 206 to receive and execute computer instructions, including those in the target program 22, and to write data and read data from the memory 206.**

The Examiner finds no evidence that the processor model shell “does not emulate the processor’s functionality.” Profit explicitly discloses that the processor model shell converts a sequence of processor functions, which correspond to an instruction executed in the target program by processor 204, into activity at the simulated pins of the target processor. The hardware simulator of Profit clearly contains a virtual microcontroller, specifically processor model shell 212.

To address Applicants’ second argument, Applicants’ attention is respectfully drawn to Profit, column 5, lines 51-57:

**The system of the present invention also allows the extensive use of existing debugging tools to aid the developer in the development and integration of the target system. The system combines interacting elements of hardware and executing software, in part by physical emulation and in part by abstract software simulation.**

The Examiner finds no evidence that Profit fails to disclose “In-Circuit Emulation debug software”. Profit clearly discloses an in-circuit emulation system [*interacting elements of hardware and executing software, in part by physical emulation and in part by abstract software simulation*] to be used with existing debugging tools. Clearly Profit is disclosing the use of existing debugging tools to be used with the disclosed in-circuit emulation system. Applicants’ have neither disclosed nor claimed a particular invention specifically related to “In-Circuit Emulation debugging software,” and the Examiner can find no credible distinction between Profit’s disclosure of debugging tools and Applicants’ claimed “In-Circuit Emulation debugging software.”

Applicants’ arguments have been fully considered but have been found unpersuasive.

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Regarding claim 2, Profit teaches a gatekeeper clock running independent of the microcontroller clock to clock operations carried out in the gatekeeper circuit (column 10, lines 38-41, “In this embodiment, the simulation time keeper circuit 232 includes a counter”; column 10, lines 44-45, “The counter is driven by the clock signal on line 242”).

Regarding claim 4, Profit teaches that the gatekeeper circuit comprises means for halting the microcontroller, functionally equivalent to “holding a reset”, when a watchdog event occurs (column 8, line 65 – column 10, line 31; column 10, line 32 – column 11, line 7; especially column 9, lines 41-46).

Regarding claims 5 and 6, Profit teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring “the data address and status lines on the target bus 208 of the processor emulator 202” (column 10, lines 4-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants’ invention, in combination with his own knowledge of the particular art as well as Profit’s explicit teaching of the advantages of various embodiments, to combine and modify the teachings of Profit to arrive at the claimed invention.

Regarding the limitations specific to claim 8, Profit teaches that the gatekeeper circuit comprises means for halting the microcontroller, functionally equivalent to “holding a reset”, when a watchdog event occurs (column 8, line 65 – column 10, line 31; column 10, line 32 – column 11, line 7; especially column 9, lines 41-46).

Regarding the limitations specific to claims 9 and 10, Profit teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring “the data address and status lines on the target bus 208 of the processor emulator 202” (column 10, lines 4-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants’ invention, in combination with his own knowledge of the particular art as well as Profit’s explicit teaching of the advantages of various embodiments, to combine and modify the teachings of Profit to arrive at the claimed invention.

Regarding claim 11, Profit teaches an in-circuit emulation system with a gatekeeper circuit (referred to as RUN/HALT controller 240) (Fig. 8, reference 240; column 8, line 65 – column 10, line 31) that detects when a watchdog timer (referred to as time keeper circuit 232) expires in the microcontroller and notifying the host computer that the watchdog event has occurred (column 10, line 32 – column 11, line 7).

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Profit also teaches that the gatekeeper circuit comprises means for halting the microcontroller, functionally equivalent to “holding a reset”, when a watchdog event occurs (column 8, line 65 – column 10, line 31; column 10, line 32 – column 11, line 7; especially column 9, lines 41-46).

Profit also teaches sending a signal to the virtual microcontroller to resume its operation, functionally equivalent to providing a clock signal (column 10, lines 4-23).

Profit does not explicitly recite “permitting the host computer to query memory locations and registers of the virtual microcontroller”, however Profit does explicitly recite that the host computer contains software debugging tools (column 6, lines 49-60). It would have been obvious to a person of ordinary skill in the art at the time of Applicants’ invention to combine Profit’s explicit suggestion, in combination with his own knowledge of the particular art, to include the memory and register probing means that are both well known in the art and necessary to adequately debug software for the microcontroller.

In response, Applicants’ reiterate the arguments submitted regarding claim 1, which have been addressed above. These arguments have been fully considered but have been found unpersuasive.

Regarding claims 12 and 13, Profit teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring “the data address and status

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lines on the target bus 208 of the processor emulator 202” (column 10, lines 4-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants’ invention, in combination with his own knowledge of the particular art as well as Profit’s explicit teaching of the advantages of various embodiments, to combine and modify the teachings of Profit to arrive at the claimed invention.

Regarding claim 14, Profit teaches a gatekeeper clock running independent of the microcontroller clock to clock operations carried out in the gatekeeper circuit (column 10, lines 38-41, “In this embodiment, the simulation time keeper circuit 232 includes a counter”; column 10, lines 44-45, “The counter is driven by the clock signal on line 242”).

Regarding claim 15, Profit teaches an in-circuit emulation system with a gatekeeper circuit (referred to as RUN/HALT controller 240) (Fig. 8, reference 240; column 8, line 65 – column 10, line 31) that detects when a watchdog timer (referred to as time keeper circuit 232) expires in the microcontroller and notifying the host computer that the watchdog event has occurred (column 10, line 32 – column 11, line 7).

Profit also teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring “the data address and status lines on the target bus 208 of the processor emulator 202” (column 10, lines 4-6). It would have been obvious to a person of

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ordinary skill in the art at the time of Applicants' invention, in combination with his own knowledge of the particular art as well as Profit's explicit teaching of the advantages of various embodiments, to combine and modify the teachings of Profit to arrive at the claimed limitation of "determining that a watchdog timer event has occurred in a microcontroller".

Profit also teaches a virtual microprocessor (referred to as a processor model shell 212) (column 6, lines 25-32) running in lock-step with the microprocessor (column 11, lines 40-43);

Profit also teaches that the gatekeeper circuit comprises means for halting the microcontroller, functionally equivalent to "holding a reset", when a watchdog event occurs (column 8, line 65 – column 10, line 31; column 10, line 32 – column 11, line 7; especially column 9, lines 41-46).

Profit also teaches notifying a host computer running in-circuit emulation software that a watchdog timer event has occurred (column 11, lines 56-61).

In response, Applicants' reiterate the arguments submitted regarding claim 1, which have been addressed above. These arguments have been fully considered but have been found unpersuasive.

Regarding claim 16, Profit does not explicitly recite "permitting the host computer to query memory locations and registers of the virtual microcontroller", however Profit does explicitly recite that the host computer contains software debugging tools (column 6, lines 49-60). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine Profit's explicit suggestion, in combination with his own knowledge of the

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particular art, to include the memory and register probing means that are both well known in the art and necessary to adequately debug software for the microcontroller.

Regarding claims 17 and 18, Profit teaches that the gatekeeper circuit (RUN/HALT controller 240) detects that a watchdog event has occurred by monitoring the state of the microcontroller (column 9, lines 47-55). In another embodiment, Profit teaches that the target bus watch circuit 224 (which comprises, among other components, the RUN/HALT controller 240) detects when a watchdog event has occurred by monitoring “the data address and status lines on the target bus 208 of the processor emulator 202” (column 10, lines 4-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants’ invention, in combination with his own knowledge of the particular art as well as Profit’s explicit teaching of the advantages of various embodiments, to combine and modify the teachings of Profit to arrive at the claimed invention.

Regarding claim 19, Profit teaches a gatekeeper clock running independent of the microcontroller clock to clock operations carried out in the gatekeeper circuit (column 10, lines 38-41, “In this embodiment, the simulation time keeper circuit 232 includes a counter”; column 10, lines 44-45, “The counter is driven by the clock signal on line 242”).

*Conclusion*

Applicant's amendment and arguments necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

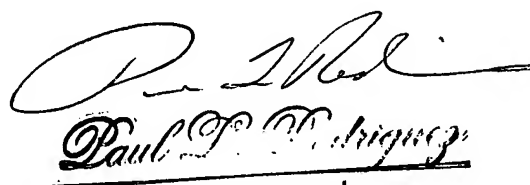
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor  
Examiner  
Art Unit 2123

jsp

  
Paul J. M. Arizaga  
Primary Examiner  
Art Unit 2125